

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7560	(717/155,157;703/2,14,21;716/1-5,11-14,18).cccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/09 15:35
S1	6862	((717/151-155) or (716/1,3-5,7,11,13,18) or (703/2,14,21,23)).CCLS.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2004/08/07 13:33
S3	5	S1 and netlist and HDL and synthesis and speculation and pipelin\$4 and block and (sharing or shared) and (expression same function)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/07 13:36
S4	592	(@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4) and ((hardware and software) same (lay\$4 or set\$4 or configur\$4 or mapp\$4)) and compiler	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:01
S5	2025	(HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 11:59
S6	50	HDL same pipelin\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 12:59
S7	7	(HDL same pipelin\$4) and (@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4) and (hardware same software) and compiler	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 13:00
S8	3	(HDL same pipelin\$4) and (@ad<="20000807" or @rlad<="20000807") and runtime and (hardware same software) and compiler	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 13:00
S9	14	(HDL same pipelin\$4) and (@ad<="20000807" or @rlad<="20000807") and (hardware same software) and compiler	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 13:00

S10	67	((@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4) and ((hardware and software) same (lay\$4 or set\$4 or configur\$4 or mapp\$4)) and compiler) and ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 13:01
S11	6	(((@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4) and ((hardware and software) same (lay\$4 or set\$4 or configur\$4 or mapp\$4)) and compiler) and ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4))) and (HDL same pipelin\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:03
S12	127	(mapp\$4 or translat\$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 14:04
S13	2025	(HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 14:05
S14	18	((mapp\$4 or translat\$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware )) and ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4) )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 14:05
S15	7	((((mapp\$4 or translat\$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware )) and ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4) )) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 15:42
S16	40	((flow or expression or pointer and array) same (hardware adj2 (circuit\$5 or resource or entity or line or gate))) and compil\$4 and (RTL or synthesis or (hardware adj2 definition))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 14:57

S17	27	((flow or expression or pointer and array) same (hardware adj2 (circuit\$5 or resource or entity or line or gate))) and compil\$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:50
S18	6	"5650948".URPN.	USPAT	OR	ON	2004/08/05 15:15
S19	6	"5650948".URPN.	USPAT	OR	ON	2004/08/05 15:15
S20	3	(speculat\$4 and (block neare3 shar\$4) and (loop near3 pipeline) and compiler and ((synthesis same hardware) or (HDL or Verilog or PLA or FPGA or cosimulation))) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 15:46
S21	4	speculat\$4 and (block neare3 shar\$4) and (loop near3 pipeline) and compiler and ((synthesis same hardware) or (HDL or Verilog or PLA or FPGA or cosimulation))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 15:45
S22	5	speculat\$4 and (block neare3 shar\$4) and (loop near3 pipeline) and compiler and ((synthesis or HLS) or (HDL or Verilog or PLA or FPGA or cosimulation or SystemC))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:27
S23	2	(speculat\$4 and (block neare3 shar\$4) and (loop near3 pipeline) and compiler and ((synthesis or HLS) or (HDL or Verilog or PLA or FPGA or cosimulation or SystemC))) not ((speculat\$4 and (block neare3 shar\$4) and (loop near3 pipeline) and compiler and ((synthesis same hardware) or (HDL or Verilog or PLA or FPGA or cosimulation))) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 15:46
S24	1	speculat\$4 and (block neare3 shar\$4) and (loop near3 pipeline) and ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4) )	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:05
S25	1	(("flow graph" or (loop adj2 schedul\$5)) same "high-level programming") and (optimi\$5 and (hardware same (synthesis or netlist)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:08

S26	8	(((((flow or expression or pointer and array) same (hardware adj2 (circuit\$5 or resource or entity or line or gate))) and compil\$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<="20000807" or @rlad<="20000807"))) and ("high-level programming") and (optimi\$5 and (hardware same (synthesis or netlist)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:17
S27	2	"6219628".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 15:59
S28	12	("5309556"   "5497498"   "5535342"   "5541849"   "5583749"   "5603043"   "5638299"   "5652875"   "5684980"   "5732277"   "5737235"   "6064409").PN.	USPAT	OR	ON	2004/08/05 16:00
S29	74	"5541849".URPN.	USPAT	OR	ON	2004/08/05 16:04
S30	74	"5541849".URPN.	USPAT	OR	ON	2004/08/05 16:04
S31	70	((speculat\$4 and (loop near3 pipeline)) or (block neare3 shar\$4)) and ((speculat\$4 or (block neare3 shar\$4) or (loop near3 pipeline)) and "5541849".URPN.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:48
S32	10	((speculat\$4 or (modulo or pipeline))) and (((speculat\$4 and (loop near3 pipeline)) or (block neare3 shar\$4)) and ((speculat\$4 or (block neare3 shar\$4) or (loop near3 pipeline)) and "5541849".URPN.))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:35
S33	8	(pipeline and (block neare3 shar\$4)) and ((speculat\$4 or (block neare3 shar\$4) or (loop near3 pipeline)) and "5541849".URPN.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:10

S34	8	((speculat\$4 or (modulo or pipeline))) and (((speculat\$4 and (loop near3 pipeline)) or (block neare3 shar\$4)) and ((speculat\$4 or (block neare3 shar\$4) or (loop near3 pipeline)) and "5541849". URPN.))) and ((pipeline and (block neare3 shar\$4)) and ((speculat\$4 or (block neare3 shar\$4) or (loop near3 pipeline)) and "5541849". URPN.))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:10
S35	23	(block near3 sharing) and (((mapp\$4 or translat\$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware )) or ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4) ))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:35
S36	18	( (block near3 sharing) and (((mapp\$4 or translat\$4) adj3 ((software ajd2 (variable or structure or construct)) adj2 hardware )) or ((HDL or Verilog or "hardware description language") and (pipelin\$4 or schedul\$4 or speculativ\$4) ))) and (hardware same (synthesis or netlist))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:18
S37	23	(speculat\$4 or (block neare3 sharing) or (loop near3 pipeline)) and compiler and (((flow or expression or pointer and array) same (hardware adj2 (circuit\$5 or resource or entity or line or gate))) and compil\$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:26
S38	23	((speculat\$4 or (block neare3 sharing) or (loop near3 pipeline)) and compiler and (((flow or expression or pointer and array) same (hardware adj2 (circuit\$5 or resource or entity or line or gate))) and compil\$4 and (RTL or synthesis or (hardware adj2 definition))) and (@ad<="20000807" or @rlad<="20000807")) and ((synthesis or HLS or netlist) or (HDL or Verilog or PLA or FPGA or cosimulation or SystemC))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:27

S39	11	((speculat\$4 or (modulo or pipeline))) and "5541849".URPN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:41
S40	12	"5751596".URPN.	USPAT	OR	ON	2004/08/05 16:41
S41	8	((speculat\$4 or (modulo or pipeline) or (block near2 sharing))) and (netlist and synthesis)) and ( "high-level programming") and ((optimi\$5 or mapping) (hardware same (software or programming or RTL) ))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:43
S42	26	((speculat\$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 11:04
S43	22	((speculat\$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:51
S44	13	((speculat\$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<="20000807" or @rlad<="20000807")) and ("717"/\$ or "716"/\$ or "703"/\$ or "711"/\$ or "710"/\$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:52
S45	4	((speculat\$4 and (loop near3 pipeline)) or (block near sharing)) and (((speculat\$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<="20000807" or @rlad<="20000807")) and ("717"/\$ or "716"/\$ or "703"/\$ or "711"/\$ or "710"/\$)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:58
S46	5	(block near sharing) and (((speculat\$4 and (loop near3 pipeline)) or (block near3 sharing)) and (synthesis or netlist or HDL) and compiler) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/05 16:58

S47	216505	(VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:00
S48	5412	optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:02
S49	4915	(optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:02
S50	1	((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and ((loop near2 pipelin\$4) and (block near3 sharing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:03
S51	20	((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:21
S52	12	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:05
S53	10	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:05

S54	595	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:04
S55	487	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:11
S56	10	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (@ad<="20000807" or @rlad<="20000807")) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:05



S57	10	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807"))) and (((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807"))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:05
S58	764	((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:10
S59	44	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:10

S60	26	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:24
S61	26	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807")) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:19

S62	26	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807")) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) not (((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807")) and (((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807")) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:20
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S63	10	(((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))))) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807")) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) not ((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))))) and (@ad<="20000807" or @rlad<="20000807")) and ((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))))) and (@ad<="20000807" or @rlad<="20000807")) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))))) and Gupta.in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:20
S64	12	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (speculat\$5 and (block near3 sharing))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:22

S65	0	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (speculat\$5 and (block near3 sharing))) and (VHDL or HDL or Verilog)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:32
S66	1	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (speculat\$5 and (block near3 sharing))) and (netlist or ((hardware or circuit\$4) near6 synthesis))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:23
S67	635	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (speculat\$5 or (block near3 shared)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:25
S68	2040	(netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:29
S69	1202	((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:26
S70	15	(((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (speculat\$5 or (block near3 shared))) and (((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:26

S71	15	((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and (speculat\$5 or (block near3 shared))) and (((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807")) and (@ad<="20000807" or @rlad<="20000807"))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:30
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[illegible]

S73	73	(netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:30
S74	35	((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and (@ad<="20000807" or @rlad<="20000807")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:30
S75	1	(netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared)) and ((US-6505339-\$ or US-6226776-\$ or US-6026219-\$ or US-5764951-\$ or US-6625797-\$ or US-6608638-\$ or US-6415420-\$ or US-6519742-\$ or US-6035123-\$ or US-5819064-\$ or US-5706205-\$ or US-5696956-\$ or US-5650948-\$ or US-6389587-\$ or US-6360355-\$ or US-6219628-\$ or US-5652875-\$ or US-5541849-\$ or US-6588004-\$ or US-6505340-\$ or US-6080204-\$ or US-5870308-\$ or US-5649165-\$ or US-5896521-\$ or US-6588006-\$ or US-6678873-\$).did. or (US-6477683-\$ or US-6044211-\$). did. or (US-20010034876-\$).did.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:31



S76	0	((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and ((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and ((US-6505339-\$ or US-6226776-\$ or US-6026219-\$ or US-5764951-\$ or US-6625797-\$ or US-6608638-\$ or US-6415420-\$ or US-6519742-\$ or US-6035123-\$ or US-5819064-\$ or US-5706205-\$ or US-5696956-\$ or US-5650948-\$ or US-6389587-\$ or US-6360355-\$ or US-6219628-\$ or US-5652875-\$ or US-5541849-\$ or US-6588004-\$ or US-6505340-\$ or US-6080204-\$ or US-5870308-\$ or US-5649165-\$ or US-5896521-\$ or US-6588006-\$ or US-6678873-\$).did. or (US-6477683-\$ or US-6044211-\$).did. or (US-20010034876-\$).did.))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:31
S77	1	(optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and ((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and ((US-6505339-\$ or US-6226776-\$ or US-6026219-\$ or US-5764951-\$ or US-6625797-\$ or US-6608638-\$ or US-6415420-\$ or US-6519742-\$ or US-6035123-\$ or US-5819064-\$ or US-5706205-\$ or US-5696956-\$ or US-5650948-\$ or US-6389587-\$ or US-6360355-\$ or US-6219628-\$ or US-5652875-\$ or US-5541849-\$ or US-6588004-\$ or US-6505340-\$ or US-6080204-\$ or US-5870308-\$ or US-5649165-\$ or US-5896521-\$ or US-6588006-\$ or US-6678873-\$).did. or (US-6477683-\$ or US-6044211-\$).did. or (US-20010034876-\$).did.))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:31
S78	35	((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and (@ad<="20000807" or @rlad<="20000807")) and (VHDL or HDL or Verilog)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:33

S79	16	(((netlist or ((hardware or circuit\$4) near6 synthesis)) and (VHDL or HDL or Verilog) and (block near2 (sharing or shared))) and (@ad<="20000807" or @rlad<="20000807"))) and (VHDL or HDL or Verilog)) and (pipelin\$4 or speculat\$4)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 09:41
S80	10	((((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))))) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807"))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) not (((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807"))) and (((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))) and (@ad<="20000807" or @rlad<="20000807"))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))) and (speculat\$5 and (block near3 sharing)))))) and Gupta.in.) and "C"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 11:12

S81	10	((((((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))))) and (VHDL or HDL or Verilog)) and (@ad<="20000807" or @rlad<="20000807")) and (optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing)))) not (((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))))) and (@ad<="20000807" or @rlad<="20000807")) and (((((VHDL or HDL or Verilog) and (pointer and array) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing)))))) and (@ad<="20000807" or @rlad<="20000807")) and (((optimiz\$5 and (speculat\$5 or (loop near2 pipelin\$4) or (block near3 sharing))) and speculat\$5 or ((loop near2 pipelin\$4) and (block near3 sharing))) and (speculat\$5 and (block near3 sharing)))))) and Gupta.in.) and "C"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 11:13
S82	414	((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:06
S83	5463	(HDL or Verilog or "hardware description language") and (synthesis or netlist)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:00

S84	216506	("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:01
S85	174	(@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4 or synthesis) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and compiler	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:02
S86	368	(@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:03
S87	174	((@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4 or synthesis) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and compiler) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:03

S88	174	(@ad<="20000807" or @rlad<="20000807") and (((@ad<="20000807" or @rlad<="20000807") and (emulation or cosimulat\$4 or co-simulat\$4 or synthesis) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))) and ((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and compiler) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:03
S89	144	((@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:06
S90	144	(@ad<="20000807" or @rlad<="20000807") and (((@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:09

S91	1	((@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) and (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block))))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:04
S92	51	(((@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block)))) and ((bit near2 (first or last or one)) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:08
S94	51	(@ad<="20000807" or @rlad<="20000807") and (((@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block)))) and ((bit near2 (first or last or one)) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 ( variable near3 (declar\$3 or exist\$2 or defin\$3))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:22

S95	2	((@ad<="20000807" or @rlad<="20000807") and (((@ad<="20000807" or @rlad<="20000807") and (((bit or flag or wire) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 (variable near3 (declar\$3 or exist\$2 or defin\$3)))) and (((HDL or Verilog or "hardware description language") and (synthesis or netlist)) or (("VHDL" or "HDL" or "Verilog") and (pointer and array or variable ) and (synthesis same ( hardware or circuit\$4)) and CFG or (control adj2 (flow or block)))) and ((bit near2 (first or last or one)) near6 (indicat\$4 or represent\$3 or defin\$4)) near4 (variable near3 (declar\$3 or exist\$2 or defin\$3)))) not (Silverbrook.in.)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:19
S96	4	(netlist or synthesis and (RTL or HDL)) and (wires near3 ((defin\$4 or represent\$4) near4 variable))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:21
S97	4	(@ad<="20000807" or @rlad<="20000807") and ((netlist or synthesis and (RTL or HDL)) and (wires near3 ((defin\$4 or represent\$4) near4 variable)))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:29
S98	3	((@ad<="20000807" or @rlad<="20000807") and ((netlist or synthesis and (RTL or HDL)) and (wires near3 ((defin\$4 or represent\$4) near4 variable)))) and pars\$4	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 12:30
S99	3	(execute near5 ( block near6 speculation))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 18:12
S100	1	(execut\$4 near5 ( "in parallel" near6 speculati\$5)) and (block same (optimi\$6 or basic)) and "717"/\$	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 18:14
S102	1	(( (parallel\$5 or simultane\$5) near6 speculati\$5)) and (block same (optimi\$6 or basic)) and (Schlansker or Gupta).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2004/08/06 18:19

S17 2	28	(US-5541849-\$ or US-5649165-\$ or US-5650948-\$ or US-5652875-\$ or US-5706205-\$ or US-5764951-\$ or US-5870308-\$ or US-5896521-\$ or US-6026219-\$ or US-6035123-\$ or US-6044211-\$ or US-6080204-\$ or US-6219628-\$ or US-6226776-\$ or US-6360355-\$ or US-6385757-\$ or US-6389587-\$ or US-6415420-\$ or US-6477683-\$ or US-6505339-\$ or US-6505340-\$ or US-6519742-\$ or US-6588004-\$ or US-6588006-\$ or US-6608638-\$ or US-6625797-\$).did. or (US-6678873-\$ or US-6745160-\$). did.	USPAT	OR	ON	2005/04/08 13:56
S17 3	2	S172 and (Panchui or Killian or Ashar).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 15:24
S17 4	2	"6226776".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 13:58
S17 6	1	S172 and (Panchul).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 13:59
S17 8	3	HDL and RTL and compil\$5 and (Panchul).in.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/08 15:25
S17 9	28	(US-5541849-\$ or US-5649165-\$ or US-5650948-\$ or US-5652875-\$ or US-5706205-\$ or US-5764951-\$ or US-5870308-\$ or US-5896521-\$ or US-6026219-\$ or US-6035123-\$ or US-6044211-\$ or US-6080204-\$ or US-6219628-\$ or US-6226776-\$ or US-6360355-\$ or US-6385757-\$ or US-6389587-\$ or US-6415420-\$ or US-6477683-\$ or US-6505339-\$ or US-6505340-\$ or US-6519742-\$ or US-6588004-\$ or US-6588006-\$ or US-6608638-\$ or US-6625797-\$).did. or (US-6678873-\$ or US-6745160-\$). did.	USPAT	OR	ON	2005/04/09 11:37



S18 0	5	S179 and speculativ\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/09 11:45
S18 1	11	S179 and (loop and pipelin\$4) and HDL and optimiz\$6	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/09 11:46